Referenceless Clock Recovery Circuit with Wide Frequency Acquisition Range

Tech ID: 24851 / UC Case 2014-605-0

BRIEF DESCRIPTION

The technology is a circuit that recovers a full-rate clock signal from a random digital data signal. Properties include: achieves frequency and phase locking in a single loop and a wide acquisition range.

FULL DESCRIPTION

This invention is a full-rate referenceless clock-data recovery architecture with neither a frequency detector nor a lock detector. Its operation is instead based on the theory that if an offset (or “strobe point”) is deliberately introduced into the phase detector characteristic, the pull-in range will be enhanced as long as the initial frequency offset is the appropriate polarity. Therefore, the linear phase detector itself can function as a frequency detector with a very high capture range if the polarity of the strobe point is set appropriately, consistent with the initial oscillator frequency.

A clock signal is a timing signal that helps to coordinate the actions of circuits. Any system that requires a reference to time requires a clock signal, including data transfer and the synchronization of the circuits in a CPU. Occasionally during data transfer, information is sent without an accompanying clock signal. The corresponding clock signal or frequency must be recovered to make sense of the incoming data. To recover a clock signal from an incoming random data signal, a receiver implements a process called clock-data recovery (CDR). Conventional clock-data recovery circuits typically implement two loops: One loop, which has a large frequency acquisition range, moves the internal oscillator close to the correct frequency, and the other loop, which has a small frequency acquisition range, achieves phase locking. Having two loops requires more circuitry and dissipates more power than that of a single-loop implementation.

As an alternative to the conventional dual-loop architecture, refrenceless clock and data recovery (CDR) architectures have become more popular in industry because of their simplicity and flexibility. However, the robustness of the transition between frequency acquisition and phase locking is always a concern, particularly for the linear CDR, which has an extremely limited capture range.

UCI researchers have developed a full-rate referenceless clock-data recovery architecture whose operation is based on the deliberate introduction of an offset into the signal which has a high frequency acquisition range and requires less circuitry and power than the dual loop architecture.

SUGGESTED USES

- Communication electronics: Clock data recover

ADVANTAGES

- Higher frequency acquisition range
- Achieves frequency and phase locking in a single loop and therefore requires less circuitry and power.

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OTHER INFORMATION

CATEGORIZED AS

- **Communications**
  - Internet
  - Networking
  - Wireless
- **Computer**
  - Hardware
  - Security
  - Software
- **Engineering**
  - Engineering

PATENT STATUS

Country	Type	Number	Dated	Case
United States Of America	Issued Patent	9,525,544	12/20/2016	2014-605

PUBLICATIONS

S. Huang, J. Cao, and M. M. Green, "**An 8.2-to-10.3Gb/s full-rate linear reference-less CDR without frequency detector in 0.18µm CMOS**," 2014 *IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers*, pp. 152-153.

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RELATED CASES

2014-605-0

ADDITIONAL TECHNOLOGIES BY THESE INVENTORS

- High-Speed CMOS Ring Voltage Controlled Oscillator With Low Supply Sensitivity